AMENDMENTS

Please amend the above-identified application as follows:

In the Claims

In accordance with 37 C.F.R. § 1.121, please substitute the following clean copy text for the pending claims of the same number:

(Once amended). A circuit for detecting errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal, in a communication environment wherein the DCE interfaces the DTE to a communication channel at an interface rate determined by the DCE clocking signal, the circuit comprising:

a master clock producing a master clock signal having a frequency greater than the frequency of the DCE clocking signal;

a clock generator deriving a circuit clocking signal from said master clock signal, said circuit clocking signal having the same frequency as the DCE clocking signal;

a sample enable generator for generating a first sample enable signal at a first time and a second sample enable signal at a second time; and

a sample comparator for using said first sample enable signal, said second enable signal and said DTE data signal to determine whether the DTE data signal has undergone a transition during the time interval between said first time and said second time.

6. (Once amended). A circuit for detecting errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal, in a communication environment wherein the DCE interfaces the DTE to a communication channel, the circuit comprising:

means for producing a master clock signal having a frequency greater than the frequency of the DCE clocking signal;

means for deriving a circuit clocking signal from said master clock signal, said circuit clocking signal having the same frequency as the DCE clocking signal;

means for obtaining a first sample of said DTE data signal at a first time and means for obtaining a second sample of said DTE data signal at a second time, said second time being subsequent to said first time, the interval between said first time and said second time being less than the period of the DCE clocking signal; and

means for comparing said first sample to said second sample.

9. (Once amended). The circuit of claim 8, further comprising:

means for inverting said circuit clocking signal to produce an inverted circuit clocking signal; and

means for selecting an output signal from the group consisting of said circuit clocking signal and said inverted circuit clocking signal, in response to said selector control signal.

10. (Once amended). The circuit of claim 9, further comprising:

means for latching said DTE data signal.

11. (Once amended). A method for detecting errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal, in a communication environment wherein the DCE interfaces the DTE to a communication channel, the method comprising the steps of:

providing a master clock signal having a frequency greater than the frequency of the DCE clocking signal;

deriving a circuit clocking signal from said master clock signal, said circuit clocking signal having the same frequency as the DCE clocking signal;

obtaining a first sample of said DTE data signal at a first time and a second sample of said DTE data signal at a second time, said second time being subsequent to said first time, the interval between said first time and said second time being less than the period of the DCE clocking signal; and

comparing said first sample to said second sample.

14. (Once amended). The method of claim 13, further comprising the steps of:

inverting said circuit clocking signal to produce an inverted circuit clocking signal; and

producing an output signal that is selected from the group consisting of said circuit clocking signal and said inverted circuit clocking signal, in response to said selector control signal.

15. (Once amended). The method of claim 14, further comprising the step of:

latching said DTE data signal.

16. (Newly added). The circuit of claim 5, further comprising:

a data latch for latching said DTE data signal.

17. (Newly added). The circuit of claim 16, wherein said circuit clocking signal is used as said DCE clocking signal and said sample enable generator and said data latch are clocked by said output signal.

18. (Newly added). The circuit of claim 16, wherein said sample enable generator and said data latch are clocked by said circuit clocking signal and said output signal is used as said DCE clocking signal.

19. (Newly added). The circuit of claim 17, wherein said first enable signal is generated on the rising edge of said output signal and said second enable signal is generated an integral number of master clock signals after said first enable signal.

20. (Newly added). The circuit of claim 17, wherein said first enable signal is generated one master clock period before the rising edge of said output signal and said second enable signal is generated one master clock period after said first enable signal.

21. (Newly added). The circuit of claim 18, wherein said first enable signal is generated on the rising edge of said circuit clocking signal and said second enable signal is generated an integral number of master clock signals after said first enable signal.

22. (Newly added). The circuit of claim 18, wherein said first enable signal is generated one master clock period before the rising edge of said circuit clocking signal and said second enable signal is generated one master clock period after said first enable signal.

23. (Newly added). The circuit of claim 10, wherein said circuit clocking signal is used as said DCE clocking signal and said obtaining means and said latching means are clocked by said output signal.

24. (Newly added). The circuit of claim 10, wherein said obtaining means and said latching means are clocked by said circuit clocking signal and said output signal is used as said DCE clocking signal.

25. (Newly added). The method of claim 15, further comprising the steps of:

using said output signal as said the DCE clocking signal; and

performing said obtaining step and said latching step according to a time sequence referenced to said circuit clocking signal.

26. (Newly added). The method of claim 15, further comprising the steps of:

using said circuit clocking signal as said DCE clocking signal; and

performing said obtaining step and said latching step according to a time sequence referenced to said output signal.